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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/040,224	01/02/2002	Ebrahim Andideh	42390P11353	2917

8791 7590 02/27/2003

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EXAMINER
LEE, HSIEN MING

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 02/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/040,224	Applicant(s) ANDIDEH, EBRAHIM	
	Examiner Hsien-Ming Lee	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-13 and 15-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-13 and 15-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Remarks

1. Applicant's request for RCE is acknowledged.

2. Application's cancellation to claims 2 and 14 is acknowledged. Claims 1, 3-13 and 15-30 are pending in the application.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3-9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andideh et al. (US 6,448,185) in view of Usami (US 6,222,269).

In re claims 1, 4, 6 and 7, Andideh et al. in Figs. 1a-1i and related text, teach the claimed method of forming a semiconductor device comprising:

- forming a first patterned conductive layer 101 on a dielectric material on a substrate 100, wherein the substrate can include a dielectric material on a substrate (col.2, lines 39-43)(Fig.1b);
- forming a first barrier layer 102 on the surface of the first patterned conductive layer 101 (Fig.1b);
- forming a dielectric layer 103 on the surface of the first barrier layer 102 (Fig.1b); and

- forming one of a via 107 and a trench 106 through a first portion of the dielectric layer 103 and through a first portion of the first 102 barrier layers (Fig.1h); wherein the via 107 is filled with a sacrificial light absorbing material 104, which is a dyed spin-on glass having dry etch properties similar to the dielectric layer (col.3, lines 38-53).

In contrast, Andideh et al. do not teach forming a second barrier layer on said first barrier layer; and forming said one of said via and said trench through said second barrier layer followed by forming said one of said via and said trench through said first barrier layer with a single etch process.

However, Usami in an analogous art teaches forming a first patterned conductive layer 3 on a dielectric material 2 on a substrate 1 (Fig. 2D); forming a first barrier layer 6 on the surface of the first patterned conductive layer 3 (Fig. 4A); forming a second barrier layer 7 on the surface of the first barrier layer 6 (Fig.4A); forming a dielectric layer 8/11 on the surface of the second barrier layer 7 (Figs. 4A); and forming a via through the first 6 and second 7 barrier layers with a single etch process (Fig.4B).

Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to include the second barrier layer and to employ the single etch process as taught by Usami over the first barrier layer of Andideh et al since by this manner it would protect said first barrier layer from over-etching while etching through said first and said second barrier layers to form said via with the single etch process. (col.8, lines 4-7, Usami)

In re claim 3 and 5, Andideh et al in view of Usami further teach claimed method comprising forming the trench 106 through a second portion of the dielectric layer 103 (Fig.1f) if the via 107 is formed through the first portion of the dielectric layer 103 (Fig.1c).

In re claims 8 and 9, Andideh et al in view of Usami teach that the first barrier layer is a silicon nitride, which is formed by a chemical vapor deposition process (col.2, lines 59-60, Andideh et al) but does not expressly teach that the thickness comprises either less than 20 nanometer (claim 8) or between 1 nanometer and 7 nanometer (claim 9).

However, the selection of the thickness of the first barrier layer (silicon nitride) is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious). In particular, Andideh et al suggest that the thickness of the barrier layer can be optimized with the considerations of functions of its diffusion inhibitation and etch-stop and the impact on the overall dielectric characteristics resulting from the combination of barrier layer and the dielectric layer. (col.2, line 65 through col.3, line 2) In this case, applicant is required to demonstrate the criticality of the claimed range, generally by showing that the claimed range would achieve unexpected relative to the prior art teaching. See M.P.E.P 2144.05 III.

In re claim 11, Andideh et al in view of Usami teach that the first barrier layer is a silicon nitride, which is formed by a chemical vapor deposition process (col.2, lines 59-60, Andideh et al)

5. Claims 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andideh et al. (US '185) in view of Usami (US '269) as applied to claims 1, 3-9 and 11 above, and further in view of Lamey et al. (US 5,045,870).

Andideh et al. in view of Usami substantially teach the claimed method as stated above except that the second barrier layer comprises less than 200 nanometers of silicon carbide, wherein the silicon carbide is deposited using any one of a plasma enhanced chemical deposition process, a chemical vapor deposition process and am atomic layer deposition process.

However, Lamely et. al. in an analogous art of forming a semiconductor device teach forming a first patterned conductive layer 19 on a dielectric material 17/15/10 on a substrate 11; forming a first barrier layer 21 comprising silicon nitride (col. 4, lines 4-5) on the surface of the first patterned conductive layer 19; forming a second barrier layer 23 comprising silicon carbide (col. 4, lines 4-5) on the surface of the first barrier layer 21, wherein the first 21 and second 23 barrier are formed by PECVD (col. 6, lines 55-57); forming a dielectric layer 25 on the surface of the second barrier layer 23; and forming a via through a first portion of the dielectric layer 17/15/10.

Therefore, at the time the invention was made, one of the ordinary skill in the art would have been motivated to modify the method of Andideh et al. in view of Usami by forming the second barrier layer using the silicon carbide as taught by Lamey et al. on the surface of the first barrier layer (silicon nitride) since by forming dual barrier layers (silicon nitride and silicon carbide) on the patterned conductive layer it would minimize the probability of pinhole-alignment directly from one film to the adjacent film, thus making a relatively impervious combined film structure. (col. 6, lines 55-64, Lamey et al.)

The combination of Andideh et al., Usami and Lamey et al. still fail to teach the claimed thickness of the silicon carbide. However, the selection of the thickness of the silicon carbide is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious). In this case, applicant is required to demonstrate the criticality of the claimed range, generally by showing that the claimed range would achieve unexpected relative to the prior art teaching. See M.P.E.P 2144.05 III.

6. Claims 13, 15-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andideh et al. (US '185) in view of Lamey et al. (US '870).

In re claim 13, 15-18 and 21-28, Andideh et al. in Figs. 1a-1i and related text, teach the claimed method of forming a semiconductor device as stated above in the rejection to claims 1, 4, 6 and 7 except forming a second barrier layer comprising silicon carbide on the surface of said first barrier layer.

However, Lamely et. al. in an analogous art of forming a semiconductor device teach forming a first barrier layer 21 comprising silicon nitride (col. 4, lines 4-5) on the surface of the first patterned conductive layer 19; forming a second barrier layer 23 comprising silicon carbide (col. 4, lines 4-5) on the surface of the first barrier layer 21, wherein the first 21 and second 23 barrier are formed by PECVD (col. 6, lines 55-57); forming a dielectric layer 25 on the surface of the second barrier layer 23; and forming a via through a first portion of the dielectric layer 17/15/10.

Therefore, at the time the invention was made, one of the ordinary skill in the art would have been motivated to modify the method of Andideh et al. by forming the second barrier layer comprising the silicon carbide as taught by Lamey et al. on the surface of the first barrier layer (silicon nitride) of Andideh et al. since by doing so it would minimize the probability of pinhole-alignment directly from one film to the adjacent film, thus making a relatively impervious combined film structure. (col. 6, lines 55-64, Lamey et al.)

In re claims 19 and 29, Andideh et al. in view of Lamey et al. fail to teach that the first barrier layer comprises between 1 nanometer and 7 nanometer of silicon nitride. However, the selection of the thickness of the first barrier layer is obvious because it is a matter of determining optimum process condition by routine experimentation as the aforementioned reason in the rejection to claim 9.

In re claims 20 and 30, Andideh et al. in view of Lamey et al. still fail to teach that the second barrier layer comprises less than 200 nanometers of silicon carbide. However, the selection of the thickness of the second barrier layer is obvious because it is a matter of determining optimum process condition by routine experimentation as the aforementioned reason in the rejection to claim10.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the

organization where this application or proceeding is assigned are 703-305-0142 for regular communications and 703-305-0142 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Hsien Ming Lee
February 20, 2003